WHAT IS CLAIMED IS:

1.   An integrated circuit for providing television functionality, comprising:

        a data transport module for receiving digital video and audio data and performing preprocessing of the data;

        an IF demodulation module for receiving and preprocessing analog television signals;

        a digital audio engine for processing digital audio signals;

        an analog audio engine for processing analog audio signals;

        a digital video engine for processing digital video signals; and a

        analog video engine for processing analog video signals, wherein said data transport module, said IF demoduation module, said digital audio engine, said analog audio engine, said digital video engine and said analog video engine are coupled through a system controller.

2.   An integrated circuit for providing television functionality, comprising:

        a plurality of input elements;

        video and graphics processing elements;

        audio processing elements;

        output interfaces; and

        a control element, wherein said plurality of input elements, said video and graphics processing elements, said audio processing elements, and said output interfaces are coupled through a system controller.

3.   The integrated circuit of claim 2, wherein said plurality of input elements comprise:

        an IF demodulator; and

        a data transport module.

4.　　　The integrated circuit of claim 3, wherein said IF demodulator comprises a digital IF demodulator.

5.　　　The integrated circuit of claim 3, wherein said IF demodulator includes an FM demodulation system for approximating $y(n)=1/x(n)$ in FM demodulation, where $x(n)=I^2(n)+Q^2(n)$.

6.　　　The integrated circuit of claim 3, wherein said data transport module includes a video data stream front end processor.

7.　　　The integrated circuit of claim 3, wherein said data transport module includes a packet substitution module.

8.　　　The integrated circuit of claim 3, wherein said data transport module includes a media processing system.

9.　　　The integrated circuit of claim 2, wherein said video and graphics processing elements comprise:

　　　　　　an analog video decoder;

　　　　　　a digital video decoder;

　　　　　　a video and graphics processing module coupled to said analog video decoder and said digital video decoder; and

　　　　　　a video encoder coupled to said video and graphics processing module.

10.　　　The integrated circuit of claim 9, wherein said analog video decoder includes a 2D adaptive comb filter.

11.　　　The integrated circuit of claim 9, wherein said digital video decoder includes an artificial time stamp module that generates pseudo MPEG information from received DV25 or DV50 digital video information.

12. The integrated circuit of claim 9, wherein said digital video decoder includes a 2D adaptive comb filter.

13. The integrated circuit of claim 9, wherein said video and graphics processing elements further comprise a 2D engine.

14. The integrated circuit of claim 9, wherein said video and graphics processing elements further comprise a 3D engine.

15. The integrated circuit of claim 9, wherein said video and graphics processing elements further comprise a combined color look-up and gamma correction system.

16. The integrated circuit of claim 9, wherein said video encoder includes a timing generator.

17. The integrated circuit of claim 9, wherein said digital video decoder includes a teletext decoder system.

18. The integrated circuit of claim 9, wherein said video encoder includes a MPAA HDTV copy protection filter system.

19. The integrated circuit of claim 2, wherein said audio processing elements comprise:
    an audio decoder; and
    an audio processor.

20. The integrated circuit of claim 19, further comprising an audio decoder digital interface coupled between a IF demodulator and said audio decoder, wherein said audio decoder digital interface provides an all digital interface and reduces signal mismatch.

21. The integrated circuit of claim 19, wherein said audio decoder includes a signal mode detection system, wherein said signal mode detection system determines a transmission mode of a broadcast signal.

22. The integrated circuit of claim 21, wherein the broadcast signal is a Japanese Broadcast Televison System Committee broadcast signal.

23. The integrated circuit of claim 19, wherein said audio decoder includes a JBTSC signal separation processor configured to receive JBTSC signals and configured to process a main channel, a sub channel and a control channel of the JBTSC signals.

24. The integrated circuit of claim 19, wherein said audio decoder includes a digital signal processor (DSP) decoder having an execution unit, an address generator and an instruction set to decode input signals, wherein said digital signal processor decoder is reprogrammable and updateable.

25. The integrated circuit of claim 2, wherein said output interfaces includes one or more of:
      an S-Video composite interface;
      a 656 interface;
      a RF modulation interface;
      a digital audio port; and
      an analog audio port.

26. The integrated circuit of claim 2, further comprising control interfaces.

27. The integrated circuit of claim 26, wherein said control interfaces include one or more of:
      a DDR-DRAM controller;
      an EJTAG module;
      peripheral interfaces; and
      an EBI interface.

28. The integrated circuit of claim 2, further comprising ancillary interfaces.

29. The integrated circuit of claim 28, wherein said ancillary interfaces include one or more of:

    a USB 2.0 interface;

    an Ethernet interface;

    a V.90 interface; and

    a SATA interface.

30. The integrated circuit of claim 2, further comprising a reset synchronization system.

31. The integrated circuit of claim 2, further comprising an I/O multiplexing system.

32. The integrated circuit of claim 2, further comprising an adaptable strapping system.

33. The integrated circuit of claim 2, further comprising a multi-channel audio interconnect system.

34. An integrated circuit, comprising:

    a digital IF demodulator for receiving and demodulating analog television signals;

    an FM modulation system for approximating $y(n)=1/x(n)$ in FM demodulation, where $x(n)=I^2(n)+Q^2(n)$;

    a video data stream front end processor for demultiplexing video signals that us both a program identifier and are multiplexed using a time division multiplexing approach;

    a packet substitution module for substituting packets into a video data stream;

    a media processing system for processing multiple program channels containing one or more data packets;

a 2D adaptive comb filter for separating luma and chroma signals within a compositie video signal;

an artificial time stamp module that generates pseudo MPEG information from received DV25 or DV50 digital video information;

a 2D engine that provides two dimensional graphics processing;

a 3D engine that provides three dimensional graphics processing;

a combined color look-up and gamma correction system that improves video graphics;

a timing generator for generating time-dependent control signals for video signals;

a teletext decoder system for processing teletext sequences;

a MPAA HDTV copy protection filter system for providing MPAA HDTV copy protection;

an audio decoder digital interface coupled between a IF demodulator and an audio decoder the provides and all digital interface and reduces signal mismatch;

signal mode detection system that determine a transmission mode of a broadcast signal; and

a digital signal processor within an audio decoder, wherein said digital signal processor is reprogrammable and updateable.